A Very High Resolution Stacked Multilevel Inverter Topology for Adjustable Speed Drives

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***Abstract*—This paper proposes a novel 49-level stacked inverter topology for drives. The 49 levels are achieved by stacking three 17-level inverters. Each of the 17-level inverter is developed by cascading a flying capacitor inverter (FC) with three capacitor fed H-bridges. The device count can be reduced by making the FC and the three cascaded H-bridges (CHBs) common to the DC link in each phase using selector switches in between them. The selector switches need to operate at fundamental frequency only. Also the devices need to block very low voltages. Hence MOSFETs can be used. This topology requires three DC sources, each of Vdc/6 only, which can be replaced with stacked batteries for electric vehicle applications. The reduction in the DC voltage requirement is achieved by using a normal symmetric six phase induction motor (IM) with parallel connection of the opposite phase windings. All the floating capacitors in the topology can be balanced irrespective of any modulation index or load power factor. Due to the high number of voltage levels, nearest level control can be used instead of pulse width modulation, which reduces the switching losses. The dv/dt during the inverter operation is also less. Detailed experimental results at different speeds of operation and during transients ensure that the novel topology can be a viable option for high power adjustable speed drives.**

***Index Terms*—Induction motor drive, Multilevel converter (MLC), Topology, Cascaded H-bridge, Flying capacitor inverter, Nearest level control (NLC).**

I. Introduction

RESEARCH in multilevel inverters (MLI) have gone a long way since the invention of neutral point clamped MLI [1]. The advantages of NPC include reduced rating of switches and improved harmonic performance. Later FC was introduced where higher number of voltage levels were attained through several charged capacitors [2]. Active NPCs (ANPC) were then introduced to equalise the losses in semi-conductor switches [3]. As the number of voltage levels are increased, NPC suffered from neutral point balancing issue and the use of additional power diodes. In FC also, the number of flying capacitors drastically increased and controlling the capacitor voltages also became complex. Cascaded H-bridge topologies were introduced which do not have the above drawbacks. But it required additional several isolated DC sources for generating higher number of voltage levels [4]. The bulky transformers associated with the front end DC supplies make it a less viable option. Many Hybrid topologies were introduced focussing on improving the number of voltage levels. In [5], a 7-level topology is developed by extending the idea of ANPCs. A reduced device count seven level hybrid topology is discussed in [6]. A 9-level MLI feeding an open ended winding IM is analysed in [7]. A 17-level inverter with single DC link, developed by cascading an FC with three CHBs is described in [8]. Also research has moved on from hexagonal space vector (SV) structure to higher number of sides like dodecagonal [9] and octadecagonal [10] SV structure which eliminates low order harmonics depending on the number of sides. To achieve a near sinusoidal voltage, topologies with very high number of voltage levels have been proposed [11], [12]. In [12], three assymetric DC sources are used and an approach using the volt second balance is used to find the switching angles to switch to the next adjacent voltage level. In [13], a real time algorithm for obtaining the switching angles is analysed for obtaining a step modulation. Similar analysis is done for multilevel converters with varying voltage steps in [14]. Both of the above algorithms do not use any look up tables. But their real time application needs to be verified for still larger number of voltage levels because the switching angles to be computed increases with increase in the number of voltage levels. In [11], a space vector approach for switching to the nearest sampled reference vector is discussed for a 11-level inverter. The counter part of this space vector approach for the nearest level switching is discussed in [15], [16] and this is commonly called as nearest level control (NLC). In [15], a high performance torque and flux control of multilevel fed IM drive is discussed which uses the nearest level switching. NLC is strictly not a modulation technique. It just switches to the pole voltage levels nearest to the sampled value of the modulating signal. Due to the large number of voltage levels, the associated error in obtaining the sampled vector is negligible. Also due to the high quality of output voltage, torque ripple is highly reduced and the drive does not require any additional filter.

A new method of generating higher number of voltage levels by stacking multilevel inverters is discussed in [18], [19] for three phase IM drives. In [18], a 9-level stacked inverter is developed by stacking two 5-level inverters through a selector switch with inherent capacitor balancing. Here each of the 5-level inverter has a DC source of Vdc/2. In [19], the stacking method to build a 49-level inverter with reduced device count is discussed. The stacking method was extended to a six phase IM drive in [20], [21]. It was shown in six

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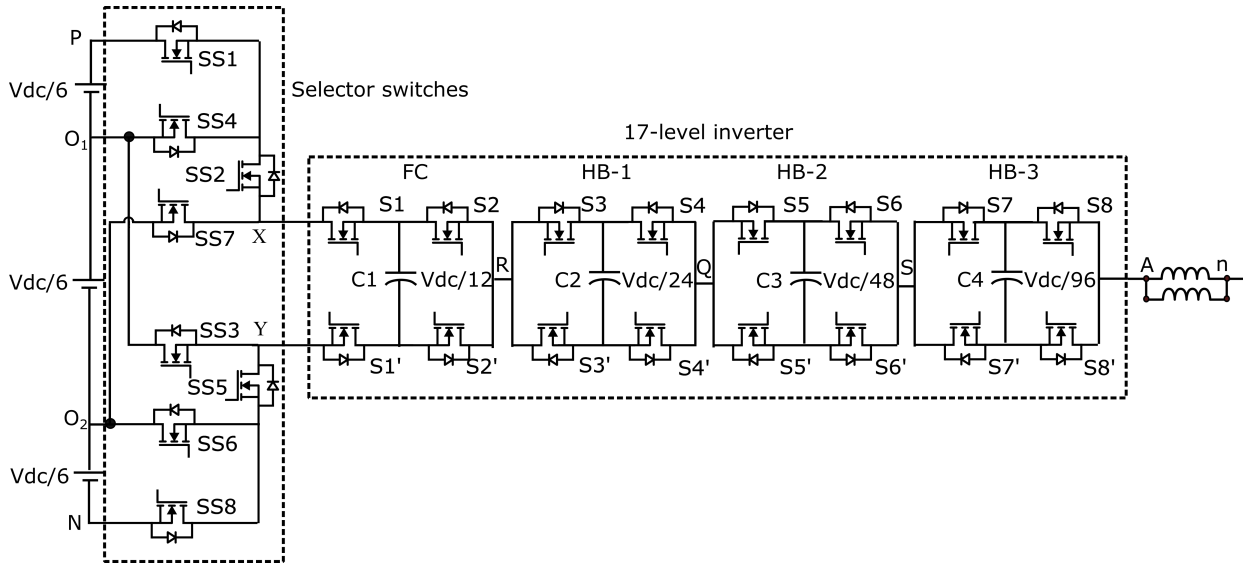


Figure 1. Reduced device count stacked 49-level inverter topology for phase 'A' by cascading an FC with three CHBs and stacking them using selector switches.

phase IM drive that a single DC source would suffice, through proper selection of switching state redundancies that ensures, in a switching interval, average mid point current becomes zero. In this research work, a novel 49-level inverter topology through stacking three 17-level inverters each of Vdc/3 (which can be reduced to Vdc/6 if a six phase machine reconfigured as a three phase machine is used) is proposed. The dv/dt associated with the inverter voltages are also very less. Due to the low voltage DC sources requirement at front end, they can be replaced with stacked batteries. It can find applications in electric vehicles. Each of the 17-level inverter is developed by cascading an FC with three CHBs [8]. For stacking, selector switches are used, which reduces the device count. The 49 levels results in a very dense space vector structure for the linear modulation range and hence the space vector location nearest to the reference space vector can be used, that is the NLC [15], [16], counterpart of the space vector approach can be used to generate the pole voltages which reduces the switching losses. Hence this drive will be very attractive for high power applications.

II. Inverter Topology and its Features

A. Stacked Operation

The stacked operation to obtain higher number of voltage levels is discussed in [18], [20] along with its various features, for three phase and six phase IM drives. The above work showed the stacked operation for two stackings. This work extends it to three stackings with three DC sources as shown in Fig. 1. The three DC sources can be reduced to Vdc/6 (instead of Vdc/3) if a six phase IM is used in a three phase winding configuration by connecting the 180 deg opposite windings in parallel configuration with appropriate polarity as shown in Fig. 2(b). This will reduce the DC link voltage requirement at front end because, for the same power output from a three phase IM and a six phase IM, a six phase machine needs only half the DC link voltage. When the DC link voltage reduces by half, the nominal voltages of the capacitors in the FC and the three CHB modules reduces by half and now MOSFETs can be used which improves the efficiency of the drive. It is to be noted that the current through each of the parallel winding (I_{a1a2} in Fig. 2(b)) is half of the respective phase current (I_a).

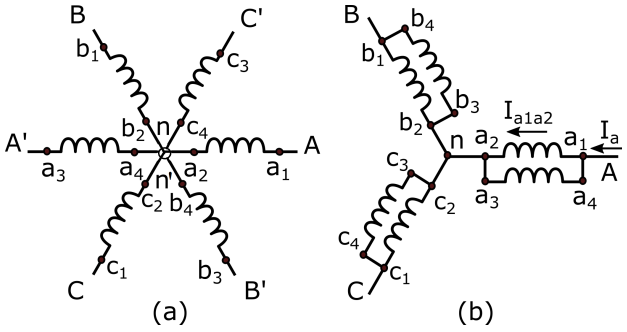


Figure 2. (a) A symmetric six phase IM windings displaced by 60 deg. (b) Reconfigured symmetric six phase winding as a three phase winding.

As mentioned before, the 49-level inverter is developed by stacking three 17-level inverters. Each of the 17-level inverter is developed by cascading an FC with three capacitor fed H-Bridges [8]. Here to reduce the device count, the 17-level inverter is made common and the selector switch is included between the DC link and the 17-level inverter in each phase as shown in Fig.1. The four capacitors in each phase has to be maintained at Vdc/12, Vdc/24, Vdc/48 and Vdc/96. Therefore the voltage rating of the switches in FC is Vdc/6 and the voltage ratings of the switches in HB-1, HB-2 and HB-3 (shown in Fig. 1) are Vdc/24, Vdc/48 and Vdc/96 respectively. The switches S1-S1', S2-S2'.....S8-S8' operate in a complementary fashion. Therefore appropriate deadband has to be provided between them. Because of the very low voltage ratings of the switches, MOSFETs can be used which improves the efficiency significantly. The selector switches connects the 17-level inverter to the appropriate DC source of

Vdc/6 depending on the pole voltage required at any instant. The voltage rating of the selector switches is Vdc/6 for the switches SS1, SS2, SS4, SS5, SS6 and SS8 whereas switches SS3 and SS7 have to be rated for Vdc/3. The switches SS1-SS4, SS6-SS8, SS3-SS5, SS2-SS7 has to be operated in a complementary fashion. Therefore again appropriate deadband has to be provided between them.

The capacitor voltage balancing in the 17-level inverter is done using the pole voltage redundancies associated with each of the pole voltages. Each of the capacitors has a tolerance band defined within which the voltages have to lie during the operation of the inverter. Fig. 3 shows the balancing of capacitor voltages using the switching state redundancies for pole voltage of 28Vdc/96. To achieve pole voltage of 28Vdc/96, ony the middle DC source need to be used. Hence only SS4, SS2, SS5, SS6 are ON from among the selector switches during this pole voltage. Fig. 3(a) shows the discharging of C1 and C2 during pole voltage of 28Vdc/96. C1 can be charged using redundancy shown in Fig. 3(b) but it discharges C2 further. To charge C2, redundancy shown in Fig. 3(c) is used. All the other capacitors in phase 'A' are unaffected when this pole voltage is applied. Similar approach can be used to balance all the capacitors within the tolerance band in the topology. Here the capacitor voltages are balanced in one or two sampling intervals and is tightly controlled by keeping the capacitor along the flow of current or against the flow of current in every sampling interval, like in a flying capacitor topology. So only the capacitor voltage level and direction of current flow is needed to select the switching state redundancy to charge control the capacitor. Some of the references also address this issue, for low multilevel structures, as referenced in the [6], [8]. This balancing algorithm is based on the switching state redundancies of the pole voltage levels and hence valid for any operating modes of the motor or transient conditions. For the 49-level inverter, Table-I shows one of the several switching state redundancies to achieve each of the 49 pole voltage levels along with its effect on the capacitor voltages for positive direction of current flow from the inverter to the machine terminal.

The operation of the inverter is as follows. The inverter has to generate pole voltages (V_{AN}) from 0, Vdc/96, 2Vdc/96, 3Vdc/96... up to 48Vdc/96. The voltage V_{XY} is always maintained at Vdc/6 through the operation of the selector switches. So the 17-level inverter always generates pole voltages (V_{AY}) from 0, Vdc/96, 2Vdc/96....upto 16Vdc/96 with respect to Y. The potential at Y with respect to N (V_{YN}) can take three values, 0, Vdc/6 and Vdc/3 depending on the instantaneous value of the modulating signal which is explained below.

The modulating signal is scaled to peak value of 48 starting from 0. For the part of the modulating signal lying between 0 to 16, the switches SS7, SS5, SS8 are turned ON and the 17-level inverter is connected to the lower DC source (V_{O_2N}) where in V_{YN} = 0. When it ranges from 16 to 32, the switches SS4, SS2, SS5 and SS6 are turned ON, during which the 17-level inverter is connected to the middle DC source ($V_{O_1O_2}$) where in V_{YN} = Vdc/6. and for the remaining part from 32 to 48, the switches SS1, SS2, SS3 are turned ON and the 17-level inverter is connected to the upper DC source (V_{PO_1}) where in V_{YN} = Vdc/3.

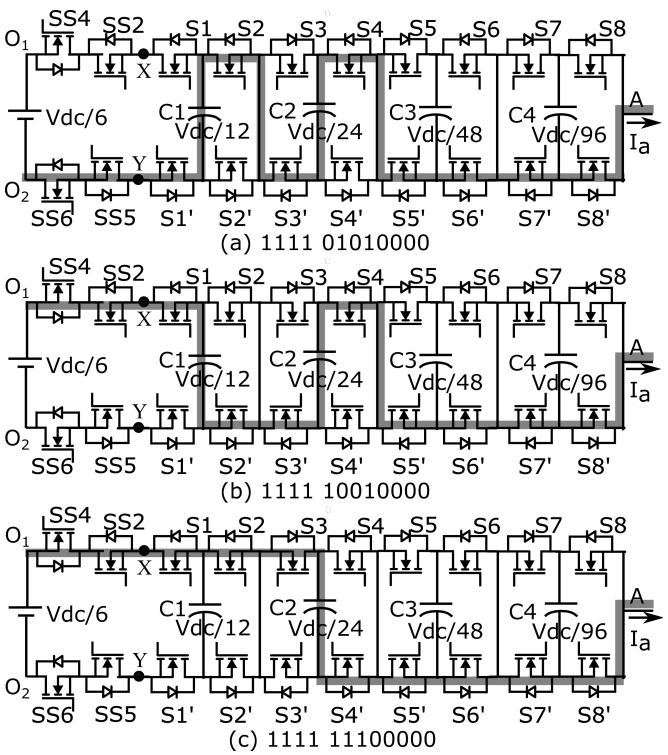


Figure 3. Capacitor voltage balancing using switching state redundancies for pole voltage of 28Vdc/96. Switching state is defined as SS4 SS2 SS5 SS6 S1 S2 S3 S4 S5 S6 S7 S8. '1' indicates switch is ON and '0' indiactes switch is OFF.

The 49-level inverter can also be developed by stacking six 9-level inverters using different arrangement of selector switches as shown in Fig. 4. Here the front end DC sources required is reduced to Vdc/12, which can be realised using stacked battery cells. Hence it will find applications in electric vehicles which are also fed from stacked battery cells.

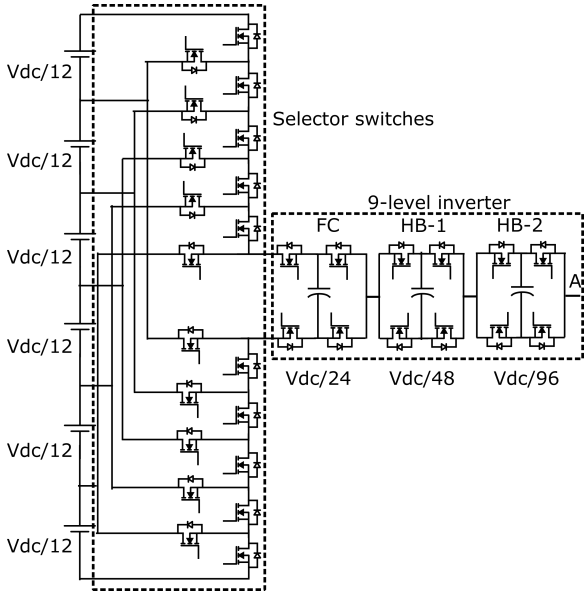


Figure 4. Reduced device count 49-level inverter developed by stacking six 9-level inverters, leading to low voltage front end DC sources of Vdc/12.

Table I
SWITCHING STATES TO ACHIEVE THE 49 POLE VOLTAGE LEVELS WITH THEIR EFFECT ON THE CAPACITOR VOLTAGES

Sl. No	V_{AN}	Switching States	C1	C2	C3	C4
1	0	11100000–00000000	U	U	U	U
2	Vdc/96	11100000–00000001	U	U	U	D
3	2Vdc/96	11100000–00000100	U	U	D	U
4	3Vdc/96	11100000–00000101	U	U	D	D
5	4Vdc/96	11100000–00010000	U	D	U	U
6	5Vdc/96	11100000–00010001	U	D	U	D
7	6Vdc/96	11100000–00010100	U	D	D	U
8	7Vdc/96	11100000–00010101	U	D	D	D
9	8Vdc/96	11100000–10000000	D	U	U	U
10	9Vdc/96	11100000–01000001	D	U	U	D
11	10Vdc/96	11100000–01000100	D	U	D	U
12	11Vdc/96	11100000–01000101	D	U	D	D
13	12Vdc/96	11100000–01010000	D	D	U	U
14	13Vdc/96	11100000–01010001	D	D	U	D
15	14Vdc/96	11100000–01010100	D	D	D	U
16	15Vdc/96	11100000–01010101	D	D	D	D
17	16Vdc/96	11100000–11000000	U	U	U	U
18	17Vdc/96	01011100–00000001	U	U	U	D
19	18Vdc/96	01011100–00000100	U	U	D	U
20	19Vdc/96	01011100–00000101	U	U	D	D
21	20Vdc/96	01011100–00010000	U	D	U	U
22	21Vdc/96	01011100–00010001	U	D	U	D
23	22Vdc/96	01011100–00010100	U	D	D	U
24	23Vdc/96	01011100–00010101	U	D	D	D
25	24Vdc/96	01011100–10000000	D	U	U	U
26	25Vdc/96	01011100–01000001	D	U	U	D
27	26Vdc/96	01011100–01000100	D	U	D	U
28	27Vdc/96	01011100–01000101	D	U	D	D
29	28Vdc/96	01011100–01010000	D	D	U	U
30	29Vdc/96	01011100–01010001	D	D	U	D
31	30Vdc/96	01011100–01010100	D	D	D	U
32	31Vdc/96	01011100–01010101	D	D	D	D
33	32Vdc/96	00001011–11000000	U	U	U	U
34	33Vdc/96	00001011–00000001	U	U	U	D
35	34Vdc/96	00001011–00000100	U	U	D	U
36	35Vdc/96	00001011-00000101	U	U	D	D
37	36Vdc/96	00001011–00010000	U	D	U	U
38	37Vdc/96	00001011–00010001	U	D	U	D
39	38Vdc/96	00001011–00010100	U	D	D	U
40	39Vdc/96	00001011–00010101	U	D	D	D
41	40Vdc/96	00001011–10000000	D	U	U	U
42	41Vdc/96	00001011–01000001	D	U	U	D
43	42Vdc/96	00001011–01000100	D	U	D	U
44	43Vdc/96	00001011–01000101	D	U	D	D
45	44Vdc/96	00001011–01010000	D	D	U	U
46	45Vdc/96	00001011–01010001	D	D	U	D
47	46Vdc/96	00001011–01010100	D	D	D	U
48	47Vdc/96	00001011–01010101	D	D	D	D
49	48Vdc/96	00001011–11000000	U	U	U	U

Note: Switch state is defined as (SS1 SS2 SS3 SS4 SS5 SS6 SS7 SS8—S1 S2 S3 S4 S5 S6 S7 S8).'1' indicates switch is ON and '0' indicates switch is OFF.

B. Nearest Level Control

Nearest level control (NLC) or its space vector counterpart is used when the number of voltage levels which the inverter can generate is quite high [15], [16]. In a conventional space vector PWM, the sampled vector is averaged out in a sampling time with the three adjacent vectors which forms the triangle, in which the tip of the sampled vector lies but when there are large number of volage levels, the space vector structure is quite dense as shown in Fig. 7 for the 49-level inverter topology and the sampled vector lies very closely to the actual space vector location. So the nearest space vector location is switched leading to only a very small stator flux ripple vector [22] which is an indication of the voltage THD. The implementation of the NLC is discussed

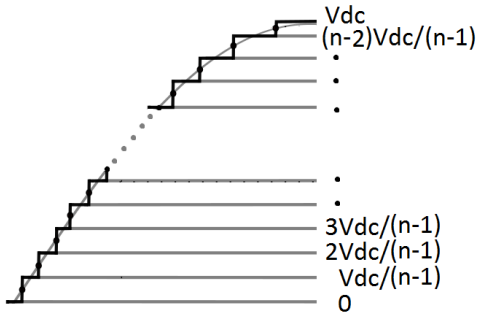


Figure 5. Nearest level control achieved by switching to the nearest available voltage level. 'n' stands for the maximum number of achievable pole voltage levels with the inverter topology

below. The sampling frequency is taken as integral multiple of the operating frequency. The samples per cycle is taken as a multiple of 6 to have both 3-phase and half wave symmetry. As mentioned before, the modulating signal is scaled from 0 to 48. The sampled modulating signal value is split into an integral and fractional part where the integral part is the lowest integer less than or equal to the sampled value. The fractional part decides whether to switch to the next adjacent voltage level or remain in the present voltage level. If the fractional part is greater than or equal to 0.5, switch to the higher voltage level or else remain in the present voltage level. Fig. 5 shows the nearest level control where the nearest pole voltage level is switched depending on the instantaneous value of the modulating signal. Depending on the pole voltage level, capacitor voltage status and the current direction, appropriate switching state redundancy is selected. This switching state redundancy ensures that the capacitor voltages are well within the tolerance band in every sampling interval. The same process is done for all the pole voltage levels using DSP and FPGA and the inverter generates the required number of pole voltage levels depending on the speed command.

C. Switching Loss

The switching loss associated with the inverter can be attributed to the losses due to the switchings in the selector switches, the FC and the three CHBs. The switchings in the selector switches are the lowest and the switchings increases from the FC to the three CHBs but the blocking voltages

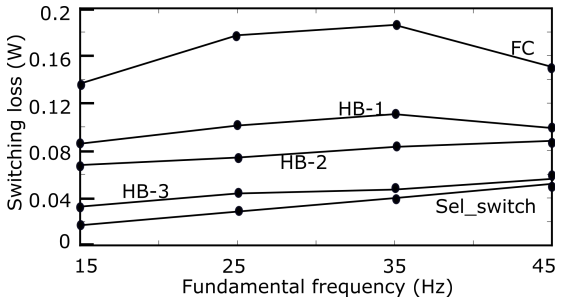


Figure 6. Selector switches, FC and the H-bridges (Fig. 1) switching losses at various frequencies of operation.

reduces by half on moving from FC to the CHBs. So the switching losses are controlled. The number of pole voltage switchings at different frequencies of operation for the selector switches, FC and the three CHBs for phase 'A' are tabulated in Table-II. The overall losses of the inverter for different frequencies are plotted in Fig. 6. Here a 7.5KW, 415V system is considered in the simulation for calculation of the switching losses with a front end DC supply of 550V. The current is taken at 10A under upf operation. The switching energy loss (E_{SW}) associated with the MOSFET can be calculated using the formulae,

$$E_{\mathrm{SW}} = \frac{V_{\mathrm{b}} * i(t)}{2} * (t_{\mathrm{S(L\text{-}H)}} + t_{\mathrm{S(H\text{-}L)}}) \quad (1)$$

V_b is the blocking volatge of the switch and i(t) is the instantaneous value of the current. The fairchild MOSFET FCH35N60 with voltage and current rating of 600V and 35A respectively is considered for the loss calculation. From the datasheet, the transition times, $t_{S(L\text{-}H)}$ and $t_{S(H\text{-}L)}$ are noted. Detailed method on how to calculate the MOSFET losses is given in [17]. E_{SW} calculated over a cycle, is divided by the fundamental period to get the power loss. It can be seen from Fig. 6 that the switching loss associated with the selector switches, which have to block the highest voltage (Vdc/6), is the least. The losses associated with the other modules are comparable since the modules with the highest switchings need to block the lowest voltage, as evident from Table-II. For reducing the conduction losses in such topologies, where the output waveforms are nearly sinusoidal with less switchings, devices with very low Rds-on like the SiC based devices have to be considered or the low cost MOSFETs can be paralleled which also result in reduced conduction losses. The heat sink design is based on the power loss of the module which dissipates the maximum losses. In the proposed scheme the stacked cells with selector switch arrangements dissipate maximum power when compared to the low voltage cascaded H- bridge modules. So the heat sink design can be based on the maximum power dissipating modules. But this can be further reduced by stacking many low voltage modules so that the voltage ratings of this stacked modules and also the conduction duration of these modules, (1/n)*T (where n is the number of stacked modules and T is the fundamental output period) will also reduce as the number of stacking increases.

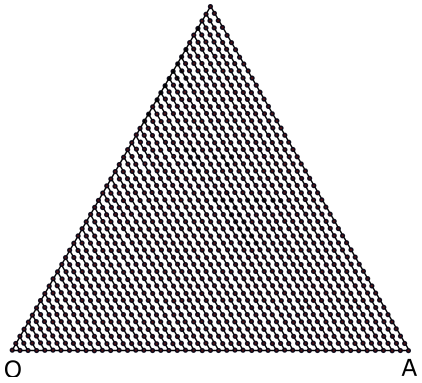


Figure 7. Highly dense space vector (SV) structure of 49-level inverter topology for 60 deg (sector-1). Dots indicate the SV locations. OA=Vdc

Table II
POLE VOLTAGE SWITCHINGS (FIG. 1) FOR PHASE 'A'

Operating frequency	Selector (V_{XN})	FC (V_{RN})	HB-1 (V_{QR})	HB-2 (V_{SQ})	HB-3 (V_{AS})
15 Hz	4	56	102	142	172
25 Hz	4	30	71	110	128
35 Hz	4	28	48	86	109
45 Hz	4	17	47	82	102

III. EXPERIMENTAL RESULTS

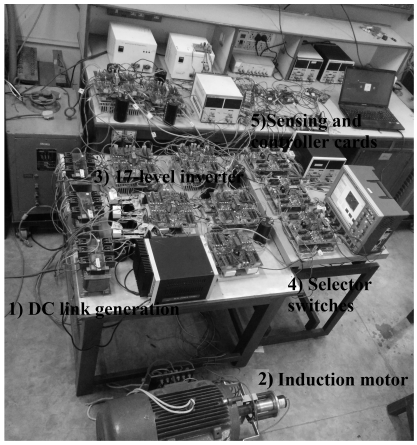


Figure 8. Laboratory prototype for the 49-level inverter topology. 1) DC link generation, 2) Induction motor, 3) 17-level inverter, 4) Selector switches, 5) Sensing and controller cards.

A symmetric 6-phase IM is driven using the 49-level inverter topology shown in Fig. 1 after configuring it as a 3-phase IM. The inverter is controlled using two DSPs (TMS320F28335) and two FPGAs (Spartan 3 XCS3200). The laboratory prototype is shown in Fig. 8. The two DSPs are synchronised and the FPGAs sends out gating pulses to the MOSFETs. Deadband of 2.5us is provided between all the complementary signals. The selector switches are controlled using DSP-1 and FPGA-1. The DSP-2 along with FPGA-2 controls the 17-level inverter. All the capacitor voltages and current directions are sensed using the ADC module in this DSP. Depending on the sensed values, digital signals are

sent out to the FPGAs which select the correct switching state stored as look up table in FPGA, based on the inputs from the DSPs. The tolerance band provided for all the flying capacitor voltages and the capacitor voltages for the CHBs are 1% around the reference values. The capacitance value, C is decided by $C = I_p T_s / \Delta V_c$, I_p is the peak load current, ΔV_c is the peak to peak voltage ripple and T_s is inverter sampling time.The experimental results are detailed below.

A. Steady State Results

The reconfigured 3-phase IM is driven with the 49-level inverter topology using V/f control scheme. Fig.9 shows the operation of the selector switches. Trace-1 shows the modulating signal with the third harmonic injection as obtained from DAC module of the DSP for 45Hz operation. Trace-2 shows the constant voltage (V_{XY}) which is same as Vdc/6. Trace-3 shows quasi square wave with the steps at magnitude of Vdc/6, Vdc/3 and Vdc/2. Fig. 10 shows the switchings

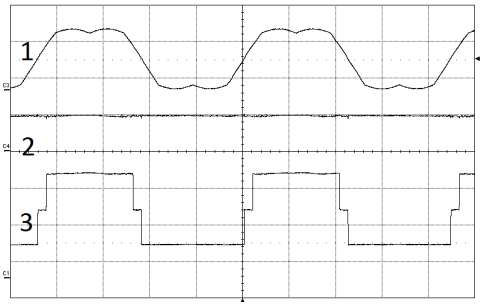


Figure 9. Operation of the selector switches (Fig. 1) at 45Hz operation. 1) Modulating signal from DAC module of DSP. 2) Constant voltage (V_{XY}) which is equal to Vdc/6, 50V/div 3) Pole voltage obtained from the operation of the selector switches (V_{XN}), 50V/div. Time scale: 5ms/div.

of the three CHBs at 45Hz operation. It should be noted that the CHB which is farthest from the DC link (HB-3), switches the most and this CHB switches block the lowest voltage (Vdc/96). The CHBs (HB-1 and HB-2) nearer to the DC link needs to block slightly higher voltages (Vdc/24 and Vdc/48) but the switchings are less. As a result the switching losses are controlled. It should be noted that the switchings in these CHBs include both for pole voltage switching as well as the switching for capacitor voltage balancing. Fig.11

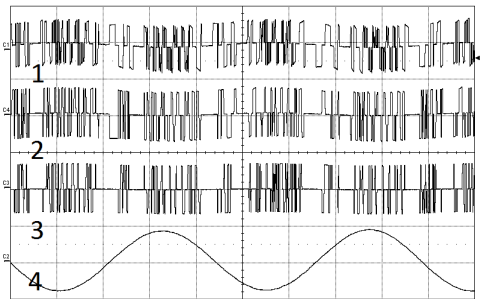


Figure 10. H-bridges (Fig. 1) switching waveforms at 45Hz operation. 1) V_{AS}, 5V/div, 2) V_{SQ}, 10V/div, 3) V_{QR}, 20V/div. 4) Phase current (I_a), 5A/div. Time scale: 5ms/div.

shows the pole voltage at different locations in the inverter at 45Hz operation. Trace-1 shows the pole voltage (V_{RN}) which is obtained equivalently as a result of stacking three FCs. Trace 2 and 3 shows the pole voltages at locations (V_{QN} and V_{SN}) which are obtained equivalently as a result of stacking three 5-level inverters and three 9-level inverters. It should be noted from trace 1, 2 and 3 that the waveform is approaching a third harmonic injected sine wave. The results at different

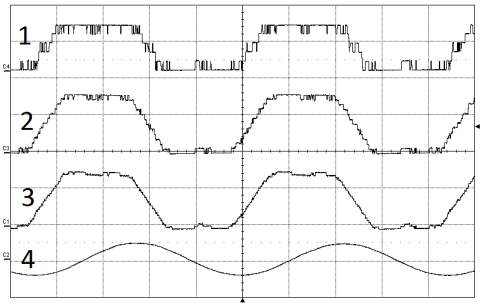


Figure 11. Pole voltages at different locations in the inverter topology (Fig. 1) at 45Hz operation. 1) V_{RN}, 100V/div, 2) V_{QN}, 100V/div, 3) V_{SN}, 100V/div, 4) Phase current (I_a), 10A/div. Time scale: 5ms/div.

steady state operating frequencies are shown in Fig. 15(a) to (d). Trace-1 in each of the above results shows the phase voltage (V_{An}). Trace-2 shows the pole voltage (V_{AN}) waveform along with the third harmonic injection. It can be seen that the number of steps in the pole voltage waveform increases as the operating frequency is increased because the number of layers in the space vector structure increases as the modulation index or the operating frequency increases. Trace-3 shows the capacitor voltage ripple which is tightly controlled within the tolerance band. Trace-4 shows the phase current (I_a).

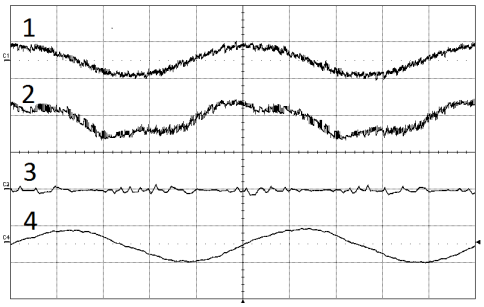


Figure 12. 10Hz waveform with adjacent vector switching. 1) Motor phase voltage (V_{An}), 50V/div 2) Inverter pole voltage (V_{AN}), 50V/div, 3) Ripple in the capacitor voltage (ΔV_{c4}), 2V/div, 4) Phase current (I_a), 10A/div. Time scale: 20ms/div.

If THD needs to be improved further at very low frequencies, the three adjacent vector switching can be used as is shown in Fig. 12 for 10Hz operation.

B. Transient Results

During the motor starting, the capacitor voltages build up without any additional precharging circuit requirement because the capacitor voltage balancing method itself ensures the correct switching state to charge up the capacitors till they comes within the tolerance band. Fig. 13 shows the same

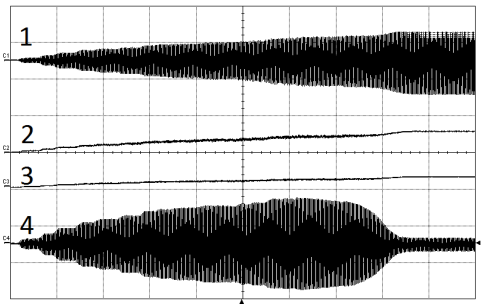


Figure 13. Capacitor voltage build up during motor starting. 1) Motor phase voltage (V_{An}), 100V/div 2) Capacitor voltage (V_{c2}), 50V/div, 3) Capacitor voltage (V_{c3}), 50V/div, 4) Phase current (I_a), 5A/div. Time scale: 1s/div.

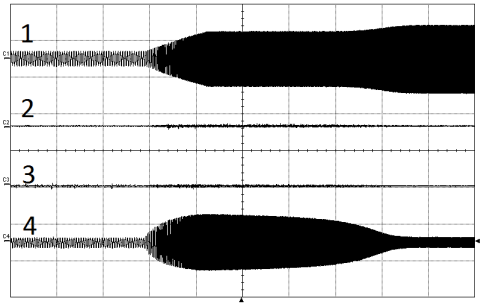


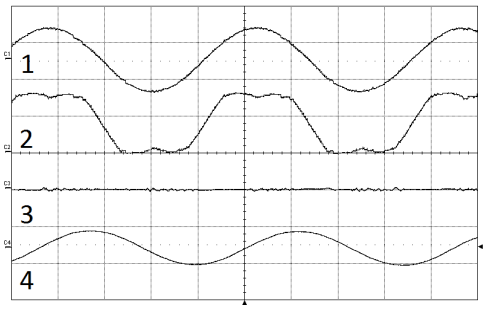
Figure 14. Motor acceleration. 1) Motor phase voltage (V_{An}), 50V/div 2) Ripple in the capacitor voltage (ΔV_{c3}), 2V/div, 3) Ripple in the capacitor voltage (ΔV_{c4}), 2V/div, 4) Phase current (I_a), 5A/div. Time scale: 1s/div.

process where the capacitors are charging up to their set values automatically during the motor start up.

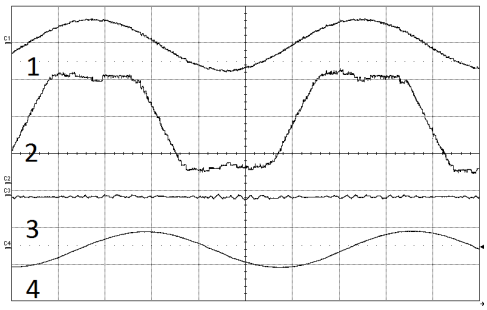
Fig. 14 shows the motor acceleration waveforms when it accelerates from 15hz to 45hz in around 4s where it can be noted that the capacitor voltages are lying within the tolerance band defined for them. The above two transient results ensure that the capacitor voltage balancing algorithm takes care of the transient conditions as well.

IV. Conclusion

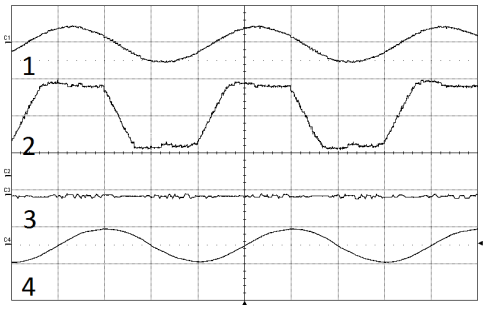
This paper proposes a novel high resolution inverter for drives applications. The higher number of voltage levels are obtained by stacking inverters with lower number of voltage levels. Here three 17-level inverters are stacked to obtain a 49-level inverter. The device voltage ratings drastically reduces and hence MOSFETs can be used which improves the efficiency of the inverter. By paralleling low cost MOSFETs or by using the SiC based devices with low Rds-on, the conduction losses can be reduced. For obtaining higher number of voltage levels, the number of stackings can be increased further and the number of cascaded H-bridges can be reduced. This will further reduce the individual DC voltage requirement at the front end. Therefore the front end DC source can be realised using stacked batteries. Thus the inverter topology can find extensive applications in electric vehicles. Nearest level control is used for switching which further reduces the switching losses associated with the MOSFETs. The capacitor voltage balancing scheme used, is independent of any modulation index or load power factor. The topology is tested for various



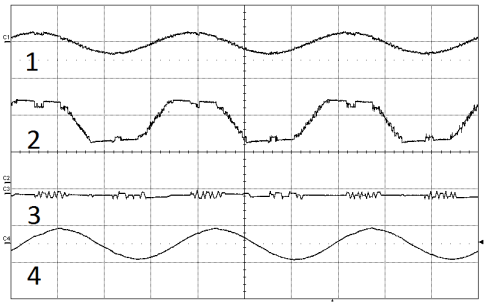
(a) 45Hz, time scale: 5ms/div



(b) 35Hz, time scale: 5ms/div



(c) 25Hz, time scale: 10ms/div



(d) 15Hz, time scale: 20ms/div

Figure 15. Steady state results for V/f operation. 1) Motor phase voltage (V_{An}), 100V/div 2) Inverter pole voltage (V_{AN}),(a)-100V/div,(b),(c),(d)-50V/div, 3) Ripple in the capacitor voltage (ΔV_{c4}), 2V/div, 4) Phase current (I_a), 10A/div, for phase 'A' for different frequencies of operation.

steady state and transient conditions and the experimental results ensure that the proposed topology is a viable option for high power IM drives.

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